AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended) An apparatus comprising:

a plurality of processors coupled to a controller and a memory;

the controller to execute a debug process, said debug process attaches at least one breakpoint bit field directly to each of a plurality of processor instructions,

wherein said controller adds at least three debug register bit fields to at least one processor control status register field, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

Claim 2 (Currently Amended) The apparatus of claim 1, wherein said at least one breakpoint bit field allows a breakpoint to be one of set and not set for each of said plurality of instructions.

Claim 3 (Original) The apparatus of claim 2, wherein a breakpoint bit set for an instruction is associated with the address of the instruction.

Claim 4 (Canceled)

Claim 5 (Currently Amended) The apparatus of ~~claim 4~~claim 1, wherein said single step field allows a set of instructions to each be single-stepped through one cycle at a time.

Claim 6 (Currently Amended) The apparatus of ~~claim 4~~claim 1, wherein said debug enable field one of enables and disables a debug mode.

Claim 7 (Currently Amended) The apparatus of claim 1, wherein at least one instruction loads content of at least one register into an instruction memory coupled to ~~said~~ at least one processor of the plurality of processors via a bus.

Claim 8 (Currently Amended) The apparatus of claim 7, wherein content of said instruction memory is loaded into a register coupled to ~~said~~ at least one processor of the plurality of processors.

Claim 9 (Original) The apparatus of claim 1, wherein internal states of each of said plurality of processors are accessible through said debug process.

Claim 10 (Withdrawn) A system comprising:

a plurality of image signal processors (ISPs), each ISP including a plurality of processor elements (PEs), the plurality of ISPs including:

a debug instruction register coupled to a first mux element,

an instruction memory coupled to an instruction register,

a decoder coupled to said instruction register,

an execution unit coupled to said decoder,

a debug executive unit coupled to said instruction memory, and

a second mux element coupled to said execution unit and a plurality of local registers,

wherein the decoder to decode at least one breakpoint bit field of each of a plurality of instructions.

Claim 11 (Withdrawn) The system of claim 10, wherein said plurality of ISPs arranged in a matrix pattern and each having quad-ports.

Claim 12 (Withdrawn) The system of claim 11, said plurality of PEs each coupled to a register file switch.

Claim 13 (Withdrawn) The system of claim 10, the decoder to decode at least three debug register bit fields of a control status register, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

Claim 14 (Withdrawn) The system of claim 13, said single step field allows a set of instructions to each be single stepped through one instruction at a time.

Claim 15 (Withdrawn) The system of claim 10, wherein at least one instruction loads content of said debug instruction register into said instruction memory.

Claim 16 (Withdrawn) The system of claim 15, wherein content of said instruction memory is loaded into said debug instruction register.

Claim 17 (Withdrawn) The system of claim 16, wherein internal states of said plurality of PEs are accessible through said debug instruction register.

Claim 18 (Currently Amended) An apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:

~~attaching~~ adding at least one breakpoint bit field directly to each of a plurality of instructions,

~~attaching~~ adding at least three debug register bit fields directly to at least one processor control status register field.

Claim 19 (Currently Amended) The apparatus of claim 18, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of said breakpoint bit, and

setting a breakpoint for an instruction if it is determined that said state of said at least one breakpoint bit field is set.

Claim 20 (Original) The apparatus of claim 18, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

Claim 21 (Original) The apparatus of claim 20, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of a run field bit, and

running a set of instructions if said state of said run field bit is set, and

stopping a set of instructions if said state of said run field bit is not set.

Claim 22 (Original) The apparatus of claim 21, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

determining a state of a single step bit,

single-stepping through a set of instructions for a cycle if said state of said single-step bit is set.

Claim 23 (Currently Amended) The apparatus of claim 18, further containing instructions which, when executed by a machine, cause the machine to perform operations including:

loading content of at least one register into an instruction memory,

loading content of said instruction memory into the at least one register, and

accessing internal states of each of a plurality of processors through ~~said~~ a debug process.

Claim 24 (Currently Amended) A method comprising:

~~attaching~~ adding at least one breakpoint bit field directly to each of a plurality of instructions,

~~attaching~~ adding at least three breakpoint register bit fields to at least one processor control status register field,

wherein the attached at least one breakpoint bit field is an additional field directly added to each processor instruction.

Claim 25 (Currently Amended) The method of claim 24, further comprising determining a state of ~~said~~ a breakpoint bit, and

setting a breakpoint for an instruction if it is determined that said state of said breakpoint bit is set.

Claim 26 (Original) The method of claim 24, further comprising:

running a debug process on a host device, and

entering debug commands through a graphical user interface.

Claim 27 (Original) The method of claim 24, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

Claim 28 (Original) The method of claim 24, further comprising:

determining a state of a single-step bit,

entering commands for single-stepping through a set of instructions for a cycle if said state of said single-step bit is set.

Claim 29 (Original) The method of claim 24, further comprising:

loading content of at least one register into an instruction memory,

loading content of said instruction memory into the at least one register, and

accessing internal states of each of a plurality of processors through said debug process, wherein accessing includes reading state values and overwriting state values.